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EXAMINER	
CONTINO, PAUL F	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,570	SEROFF, NICHOLAS CARL	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-19* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Non-Final Rejection

Response to Arguments

1. Applicant's arguments, see page 6 of the Remarks, with respect to the objection to the Drawings, have been fully considered and are persuasive. The objection to the Drawings has been withdrawn.

2. Applicant's arguments, see pages 6 and 7 of the Remarks, with respect to the rejection of claim 1 under the 102(e) reference Byrne et al., have been fully considered and are persuasive. The rejection of claim 1 has been withdrawn.

3. Applicant's arguments on page 7 of the Remarks concerning the rejection of claim 3 have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with the Applicant's arguments on page 7 regarding the failure of Byrne et al. to teach of providing controller trace data for the first and second controller. Byrne et al. teaches in column 3, lines 25-27, that controllers 12A and 12B are selectively coupled to ETM 14. Further in column 3, in lines 37-39, Byrne et al. teaches of providing trace data for the selected controller, either first controller 12A or second controller 12B. Therefor, Byrne et al. teaches that the serial trace port provides trace data for both a first and second controller.

4. Applicant's arguments, see page 7 of the Remarks, with respect to the rejection of claim 4, have been fully considered and are persuasive. The rejection of claim 4 has been withdrawn.

5. Applicant's arguments on pages 8-9 of the Remarks concerning the rejection of claims 2, 5, 6, 8-11, 13-17, and 19-23, have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with the Applicant's arguments on pages 8-9 regarding a lack of motivation to combine Byrne et al. with NS. NS states replacement of a parallel bus with a high-speed serial bus in the first paragraph of page 1. This replacement inherently allows for faster transmission of data, which in turn allows for a faster capability for debugging. Further, in the second paragraph of NS, it is discussed that serializing property of NS reduces cost, simplifies design, reduces power, and eliminates certain discrepancies in a transmission environment. The Examiner is not attempting to "convince" one skilled in the art as to why the two references should be combined, rather, to explain why one skilled in the art would have been motivated to utilize the benefits of the NS reference by implementing the NS reference itself in the Byrne et al. reference. The Examiner further respectfully disagrees that the motivation for combining the NS and Byrne et al. references were "gleaned" from the Applicant's Specification in any manner.

6. Applicant's arguments on page 10 of the Remarks concerning the rejection of claims 7, 12, and 18, have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with the Applicant's arguments on page 10 regarding a lack of motivation to combine Agarwala et al. with Byrne et al. and/or NS.

Agarwala. The Examiner further respectfully disagrees that the motivation for combining the Agarwala with the NS and Byrne et al. references were "gleaned" from the Applicant's Specification in any manner. Data compression inherently conserves the bandwidth necessary to communicate data between devices. In addition, both Agarwala et al. and Byrne et al. center around use of trace data for the debugging, which further increases the motivation to combine the references.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. (U.S. Patent No. 7,007,201) in view of Brewer et al. (U.S. Patent No. 6,886,057).

As in claim 1, Byrne et al. teaches an integrated circuit device, comprising:

a controller *(Fig. 2 #12A; column 2 lines 25-29)*; and

a serial trace port *(Fig. 2 #14/108; column 3 lines 32-43; column 5 lines 62-64; ETM 14 is interpreted as a serial trace port)*, wherein the serial trace port provides controller trace data and wherein the controller trace data is provided external to the integrated circuit device using a

serial channel *(Fig. 2; column 3 lines 34-36, where the output on 108 is interpreted as a serial channel)*.

However, Byrne et al. fails to teach of a differential serial channel. Brewer et al. teaches of a differential serial channel *(column 2 lines 1-12)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential serial channel as taught by Brewer et al. in the invention of Byrne et al. This would have been obvious because use of a differential serial bus as taught by Brewer et al. improves system performance while using a minimal amount of resources *(column 2 lines 8-12)*. Further, a differential serial bus is well-known in the art, and offers the ability to acquire data with reduced noise and disturbance due to the inverted nature of the signals, which is also why one skilled in the art would see the benefit of using a differential serial channel for communicating information.

As in claim 3, Byrne et al. discloses a second controller, wherein the serial trace port also provides controller trace data of the second controller *(Fig. 2 #12B; column 3 lines 34-36, where the selected processor 12 may be processor 12A or 12B)*.

* * *

8. Claims 2, 5, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. in view Brewer et al., further in view of NS (*SCAN921023 and SCAN921224 20-66 MHz 10 Bit But LVDS*).

As in claim 2, the combined invention of Byrne et al. and Brewer et al. teaches of a differential serial channel. However, the combined invention of Byrne et al. and Brewer et al. fails to teach of transmitting data, control and timing information in a serial stream. NS teaches of transmitting data, control and timing information in a serial stream *(page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the serial component transmission as taught by NS in the combined invention of Byrne et al. and Brewer et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which serial data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 5, Byrne et al. teaches of a trace buffer operatively coupled to the controller and the second controller *(Fig. 2 #14; column 1 lines 15-22, where the ETM is interpreted as a trace buffer)*. However, Byrne et al. fails to teach of a serializer. NS teaches of a serializer, operatively coupled between the differential serial channel and the trace buffer, which converts a parallel data stream from the trace buffer to a serial data stream for the differential serial channel *(page 1)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential transmitter as taught by NS in the invention of Byrne et al.

This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 6, Byrne et al. teaches of a trace buffer operatively coupled to the controller and the second controller *(Fig. 2 #14; column 1 lines 15-22, where the ETM is interpreted as a trace buffer)*. However, Byrne et al. fails to teach of a serializer. NS teaches of a serializer, operatively coupled between the differential serial channel and the trace buffer, which converts a parallel data stream from the trace buffer to a serial data stream for the differential serial channel *(page 1)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 8, the combined invention of Byrne et al. and NS teaches the serial trace port also provides a serializer clock signal to the serializer *(Byrne et al.: Figure 2, column 3 lines 4-5, TCK; NS: page 2; where it is interpreted that the TCK as taught in Byrne et al. provides the TCLK as taught by NS)*.

* * *

9. Claims 9, 10, 11, 13, 14, 15, 16, 17, 19, 20, 21, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. in view of NS (*SCAN921023 and SCAN921224 20-66 MHz 10 Bit But LVDS*).

As in claim 9, Byrne et al. teaches of a test apparatus, comprising:

an electronic device comprising a plurality of controllers *(Fig. 2 #12A,B; column 2 lines 25-29)*, a trace buffer operatively coupled to the plurality of controllers *(Fig. 2 #14; column 1 lines 15-22, where the ETM is interpreted as a trace buffer)*; and

a workstation, operatively coupled to the electronic device, for communicating with the electronic device *(column 1 lines 20-21, external trace port analyzer)*.

However, Byrne et al. fails to teach of a differential transmitter. NS teaches of a differential transmitter *(page 1)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 10, the combined invention of Byrne et al. and NS teaches of a serializer, operatively coupled between the differential transmitter and the trace buffer, which converts a parallel data stream from the trace buffer to a serial data stream for the differential transmitter *(NS: page 1)*.

As in claim 11, the combined invention of Byrne et al. and NS teaches of a clock means for providing clock signals to each of the plurality of controllers *(Byrne et al.: Fig. 2; column 3 lines 4-5, TCK)* and the serializer *(NS: page 2, TCLK)*.

As in claim 13, the combined invention of Byrne et al. and NS teaches of a converter operatively coupled between the electronic device and the workstation for converting data received from the electronic device to a parallel data stream for use by the workstation *(Byrne et al.: column 1 lines 20-22, external trace port analyzer; NS: page 2 figure, right side)*.

As in claim 14, the combined invention of Byrne et al. and NS teaches of transmitting data, control and timing information in a serial stream *(NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits)*.

As in claim 15, the combined invention of Byrne et al. and NS teaches the converter relays test commands from the workstation to the electronic device *(Byrne et al.: Fig. 2; column*

1 lines 20-22 and column 2 lines 37-67, where it is interpreted that the converter includes the JTAG interface and couples the JTAG device, which receives test commands from the analyzer workstation, along with the converted data stream, to the analyzer workstation).

As in claim 16, the combined invention of Byrne et al. and NS teaches of transmitting data, control and timing information in a serial stream *(NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits).*

As in claim 17, Byrne et al. teaches of a method of transforming trace data from a plurality of embedded controllers of an electronic device *(Fig. 2 #12A,B; column 2 lines 25-29)*, comprising the steps of:

storing trace data from each of the embedded controllers in memory *(Fig. 2 #14; column 1 lines 15-22, where the ETM FIFO is interpreted as memory)*;

retrieving the trace data from the memory and retrieving the trace data as a serial stream *(column 1 lines 55-56 and column 5 lines 62-64)*; and

transmitting the serial stream using at least one transmitter *(column 1 lines 19-22).*

However, Byrne fails to teach of serialization or differential transmission. NS teaches of converting data to a serial stream and transmitting the serial stream using at least one differential transmitter *(page 1).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the serialization and differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 19, the combined invention of Byrne et al. and NS teaches of receiving the transmitted serial stream and converting the received serial stream into a parallel stream *(NS: page 2 figure, right side)*; and

displaying at least a portion of the parallel stream as controller trace data *(Byrne et al.: column 1 lines 20-22, where it is interpreted that the transmitted trace data is being "displayed" to an analyzer after deserialization)*.

As in claim 20, the combined invention of Byrne et al. and NS teaches of transmitting a second serial stream using a second differential transmitter *(Byrne et al.: column 5 lines 19-25; NS: page 1; where an ETM dedicated to a single processor would necessarily use a respective differential transmitter)*.

As in claim 21, the combined invention of Byrne et al. and NS teaches the serial stream contains trace data of a first controller of the plurality of embedded controllers and the second serial stream contains trace data of a second controller of the plurality of embedded controllers

(Byrne et al.: column 5 lines 19-25; NS: page 1; where an ETM dedicated to a single processor would necessarily use a respective differential transmitter containing data of the respective processor).

As in claim 22, the combined invention of Byrne et al. and NS teaches the transmitted serial stream and the second serial stream each comprise data, control and clock information *(NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits).*

As in claim 23, the combined invention of Byrne et al. and NS teaches of transmitting data, control and timing information in a serial stream *(NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits).*

* * *

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. in view of Brewer et al., further in view of NS, further in view of Agarwala et al. (U.S. PGPub 2006/0288254).

As in claim 7, the combined invention of Byrne et al., Brewer et al., and NS teaches of a parallel data stream. However, the combined invention of Byrne et al., Brewer et al., and NS fails to teach of compressing data. Agarwala et al. teaches of a parallel data stream comprising compressed data *(Fig. 4,8,9; paragraphs [0043] and [0059]-[0066]).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the data compression as taught by Agarwala et al. in the combined invention of Byrne et al., Brewer et al., and NS. This would have been obvious because compression of data as taught by Agarwala et al. allows for faster transmission of data and conservation of inter/extra-circuit communication bandwidth.

* * *

11. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. in view of NS, further in view of Agarwala et al. (U.S. PGPub 2006/0288254).

As in claim 12, the combined invention of Byrne et al. and NS teaches of a parallel data stream. However, the combined invention of Byrne et al. and NS fails to teach of compressing data. Agarwala et al. teaches of a parallel data stream comprising compressed data *(Fig. 4,8,9; paragraphs [0043] and [0059]-[0066]).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the data compression as taught by Agarwala et al. in the combined invention of Byrne et al. and NS. This would have been obvious because compression of data as

taught by Agarwala et al. allows for faster transmission of data and conservation of inter/extra-circuit communication bandwidth.

As in claim 18, the combined invention of Byrne et al. and NS teaches of converting retrieved trace data into a serial stream. However, the combined invention of Byrne et al. and NS fails to teach of compressing data. Agarwala et al. teaches of a data stream comprising compressed data before transmission *(Fig. 4,8,9; paragraphs [0043] and [0059]-[0066])*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the data compression as taught by Agarwala et al. in the combined invention of Byrne et al. and NS. This would have been obvious because compression of data as taught by Agarwala et al. allows for faster transmission of data and conservation of inter/extra-circuit communication bandwidth.

Allowable Subject Matter

12. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
6/6/2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER